

*Fig. 1*

FIG. 2A is a schematic diagram of a first embodiment of a device. The device includes a first input terminal B1, a second input terminal B2, a first output terminal LS, and a second output terminal LS. The device includes a first switch B1, a second switch B2, a first buffer B1, a second buffer B2, a first delay element FMD, and a second delay element FMD. The first input terminal B1 is connected to the first switch B1. The second input terminal B2 is connected to the second switch B2. The first output terminal LS is connected to the first buffer B1. The second output terminal LS is connected to the second buffer B2. The first delay element FMD is connected between the first switch B1 and the first buffer B1. The second delay element FMD is connected between the second switch B2 and the second buffer B2. The first switch B1 and the second switch B2 are controlled by a common control signal. The first buffer B1 and the second buffer B2 are controlled by a common control signal. The first delay element FMD and the second delay element FMD are controlled by a common control signal.

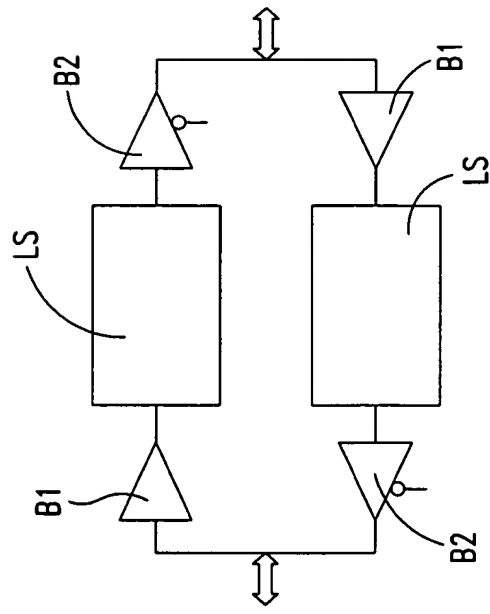


Fig. 2A

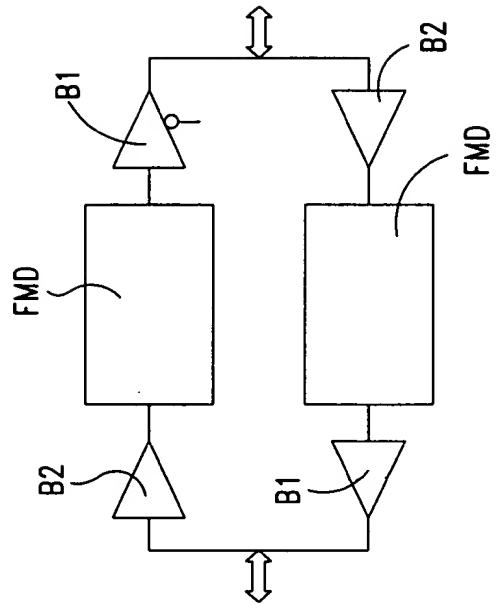


Fig. 2B

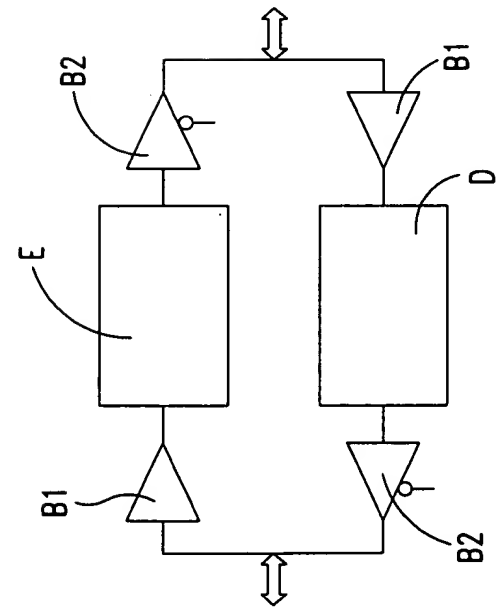


Fig. 2C

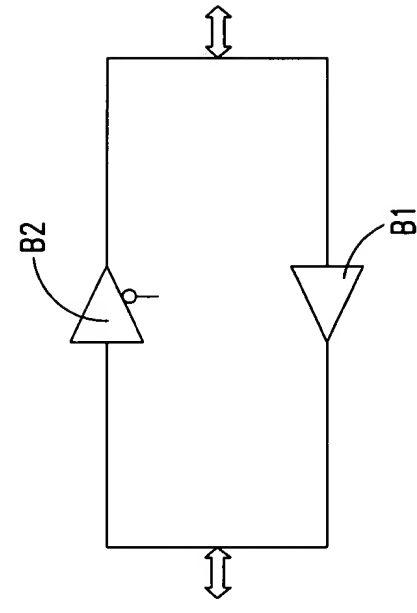
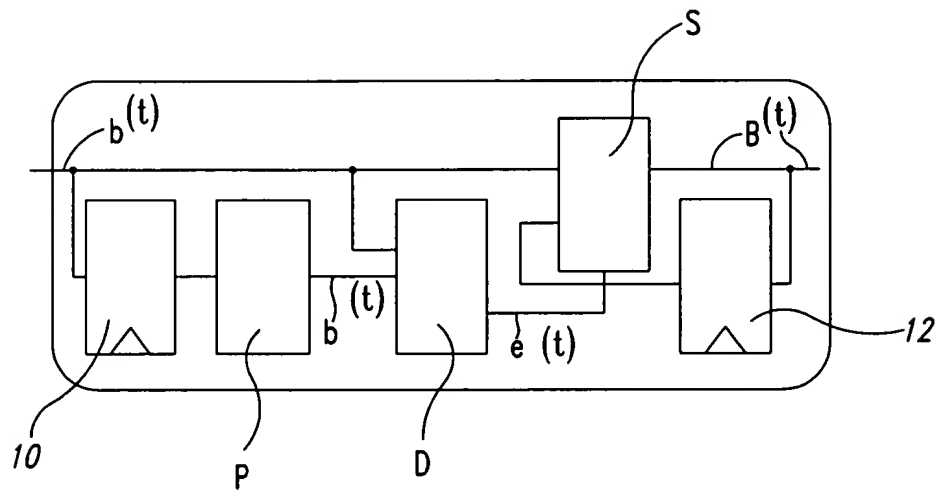
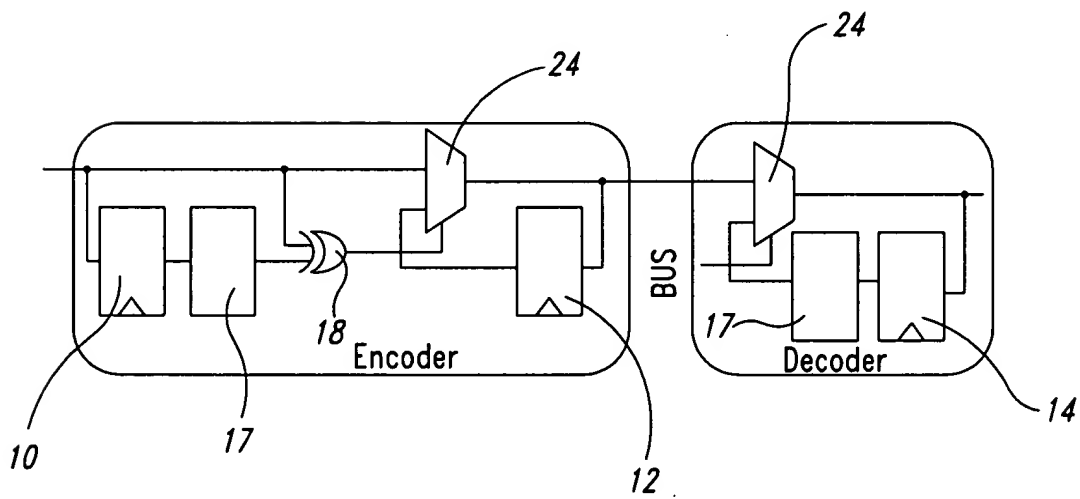


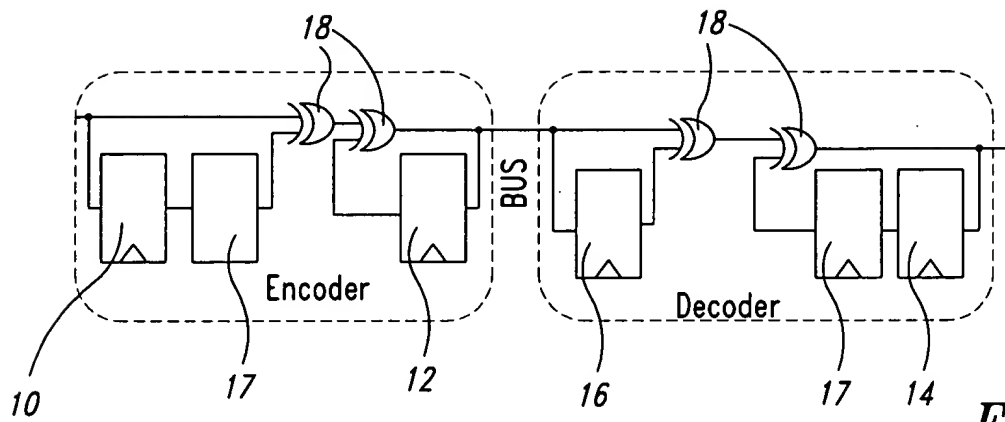
Fig. 2D



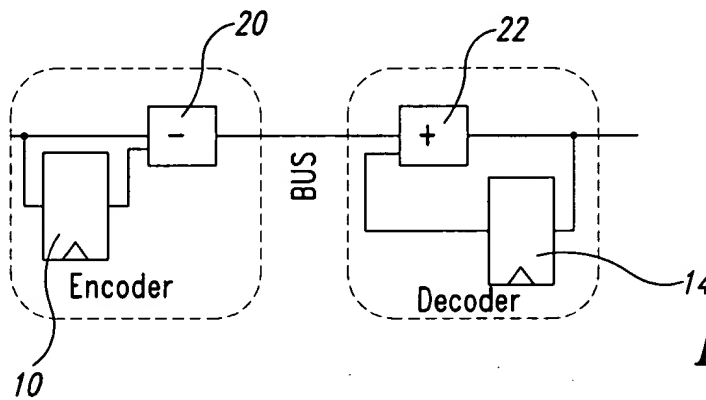
*Fig. 3*



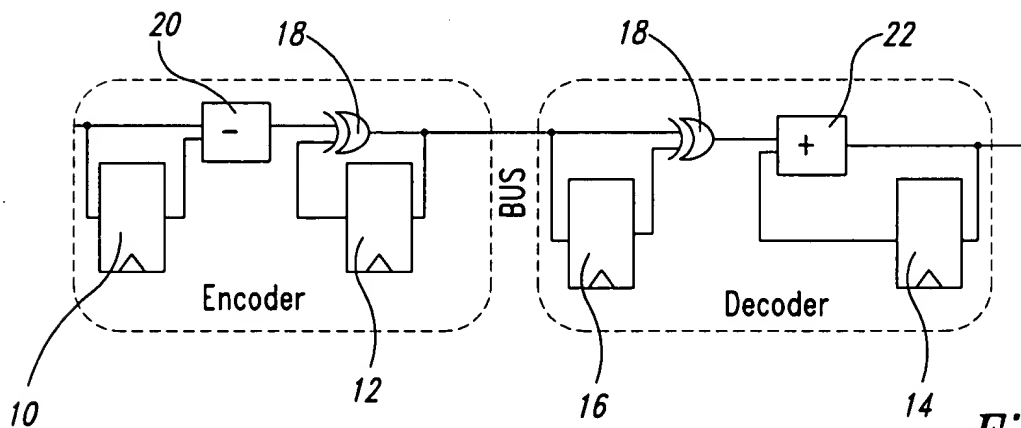
*Fig. 4*



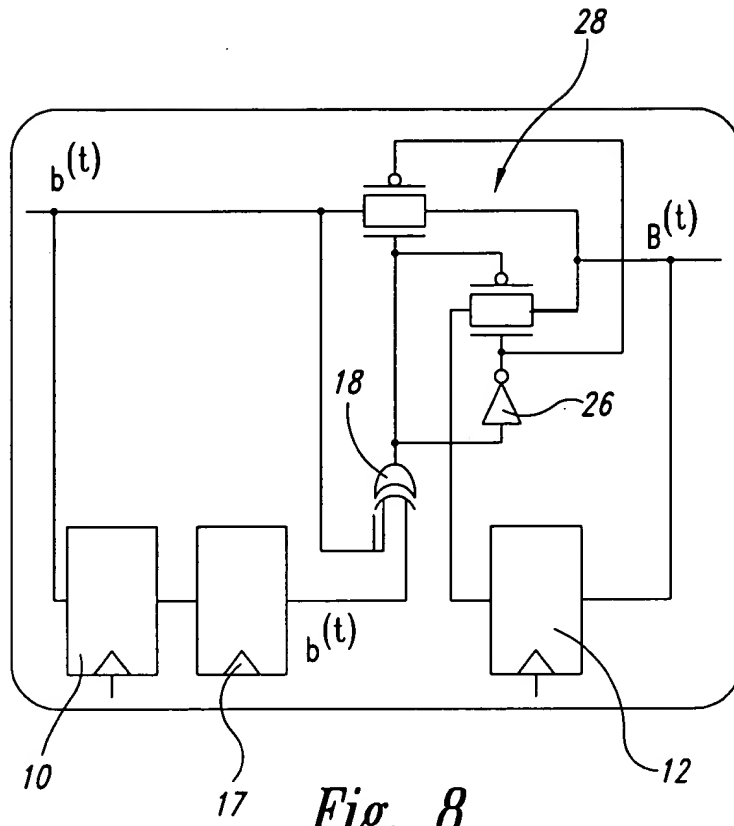
*Fig. 5*



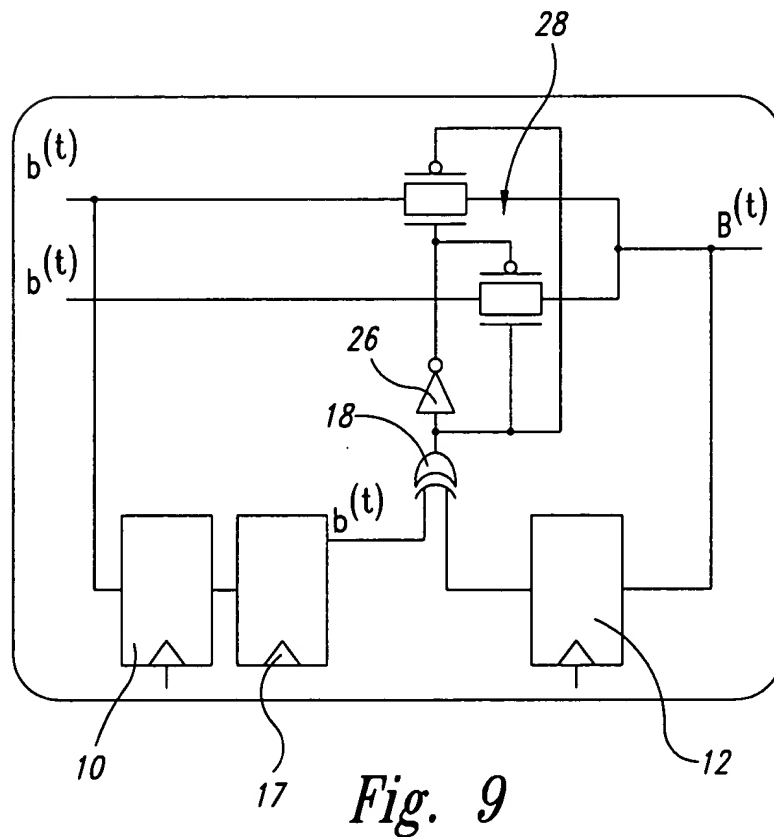
*Fig. 6*



*Fig. 7*



*Fig. 8*



*Fig. 9*